

FIG.1
CONVENTIONAL ART

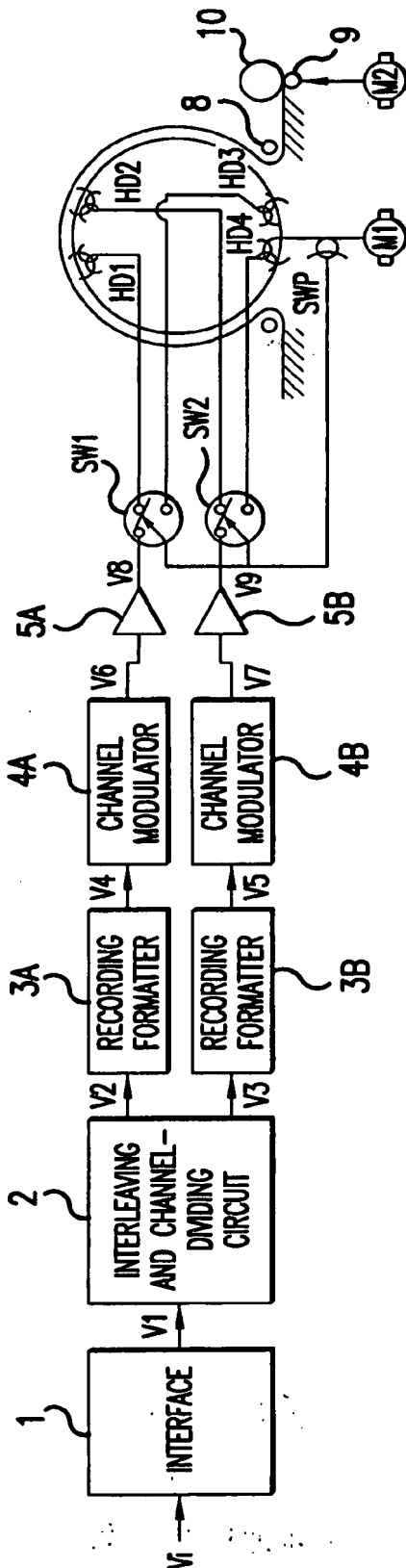


FIG.3
CONVENTIONAL ART

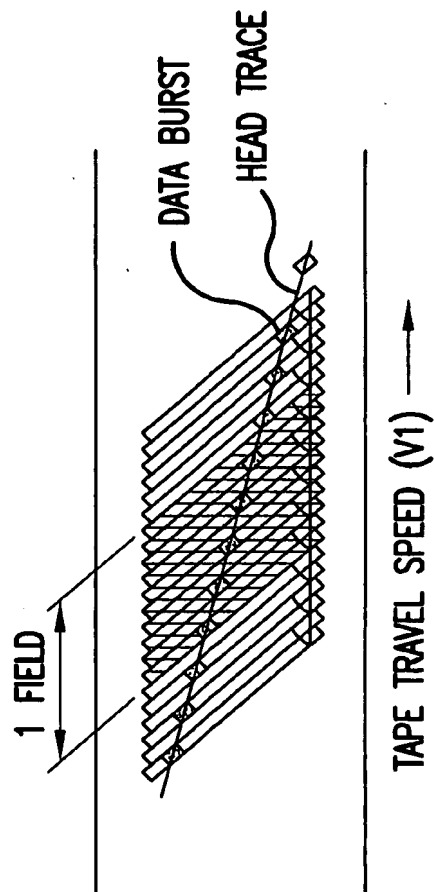
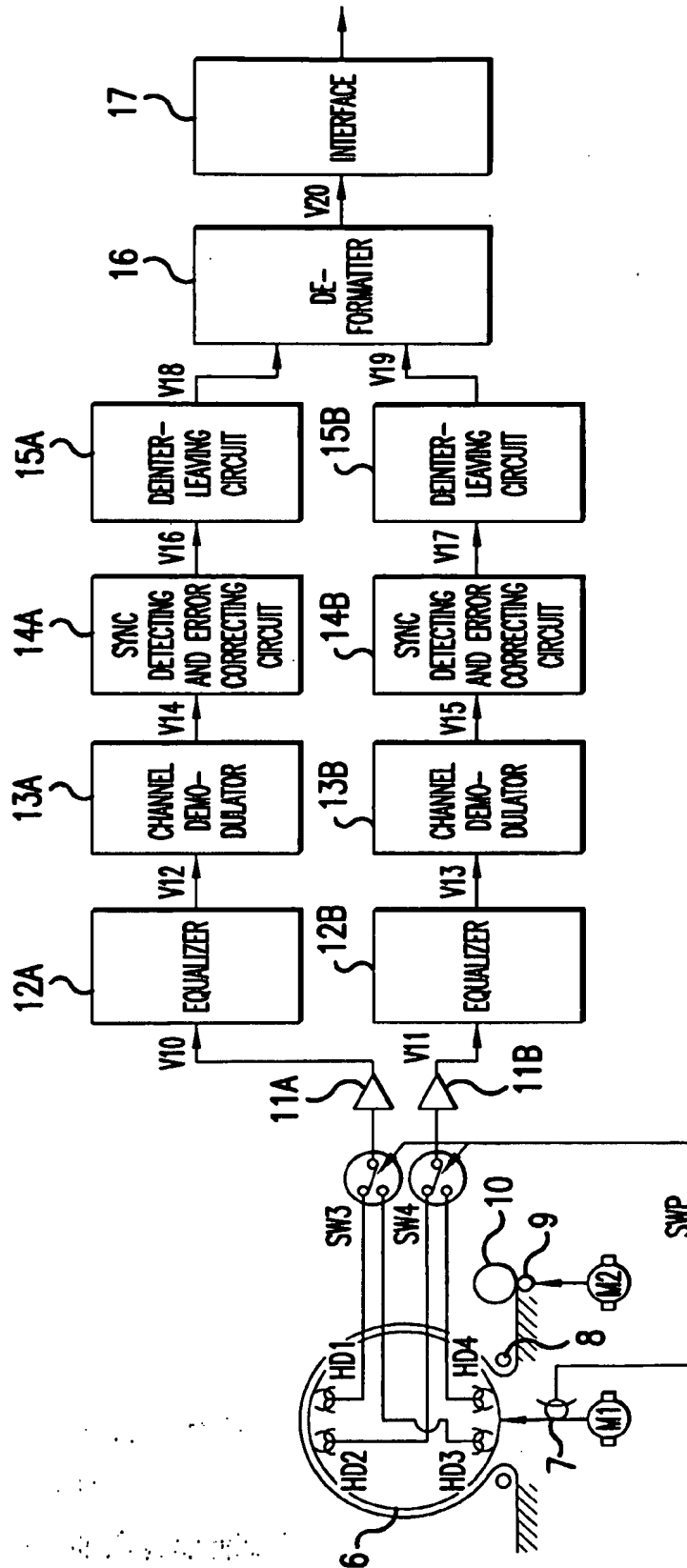
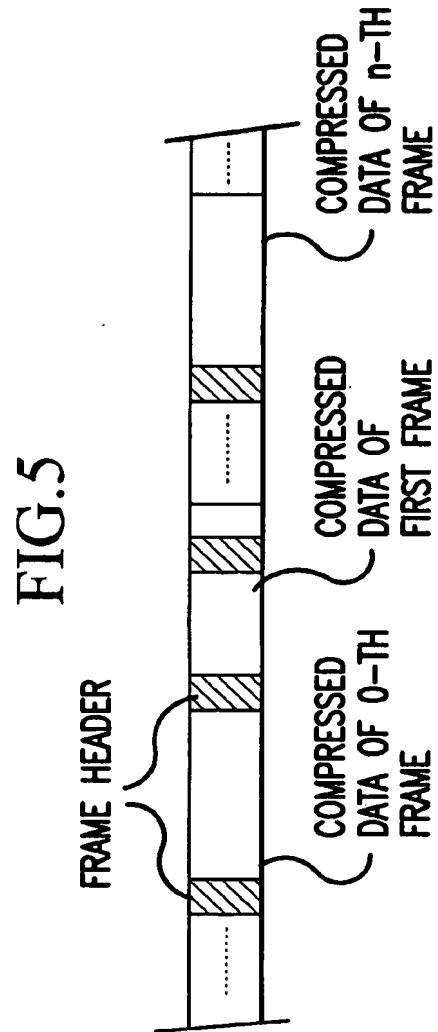
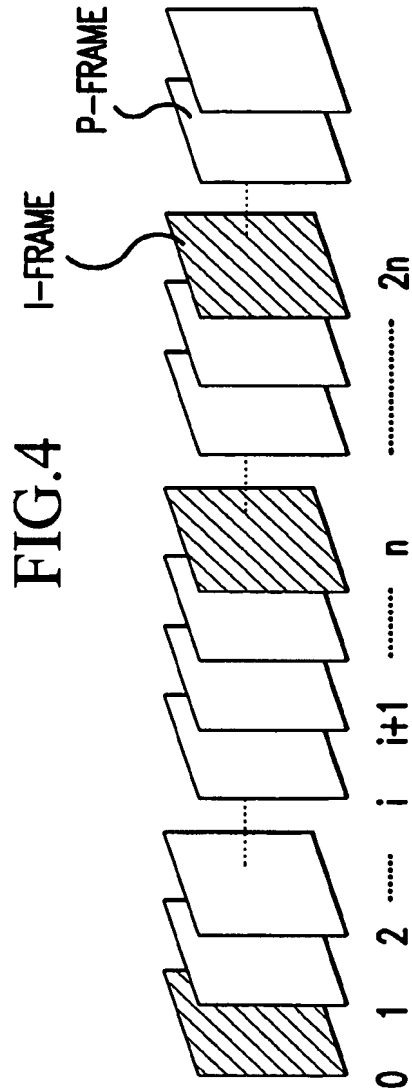


FIG.2
CONVENTIONAL ART







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FIG.6

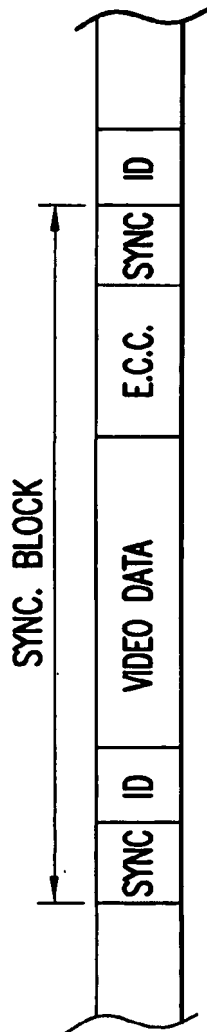
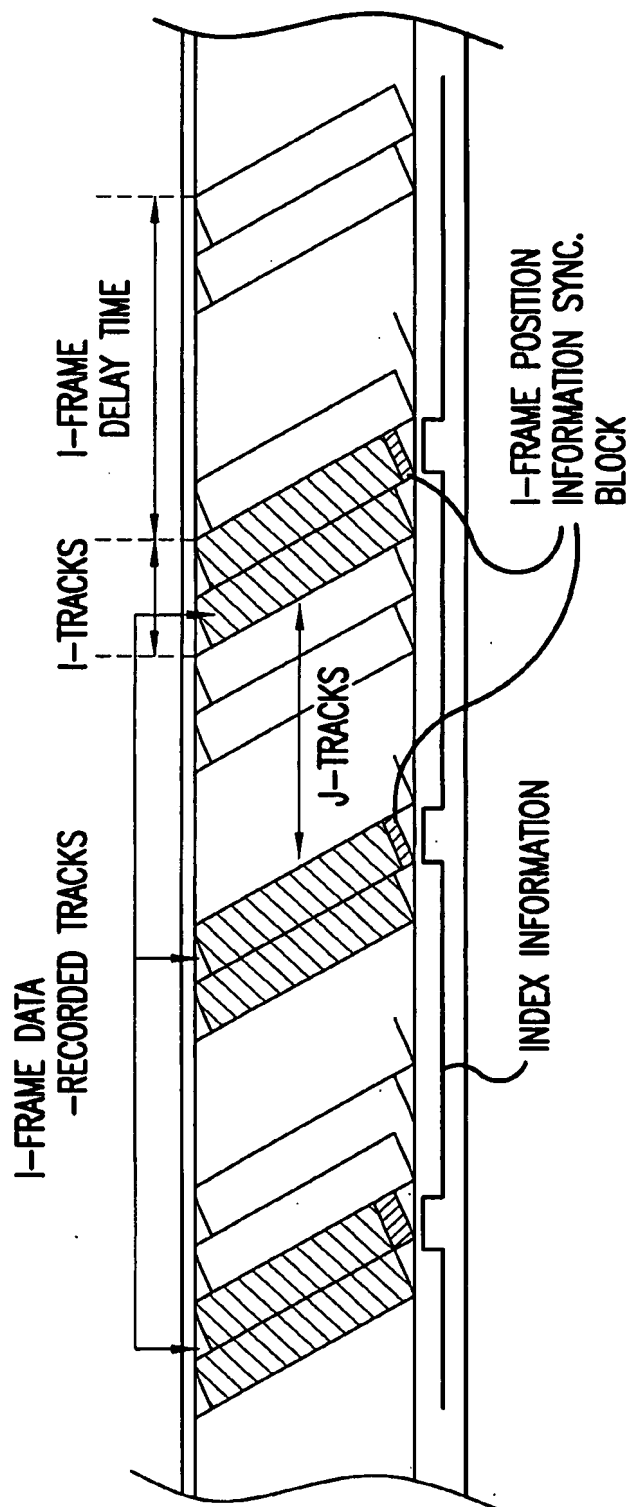
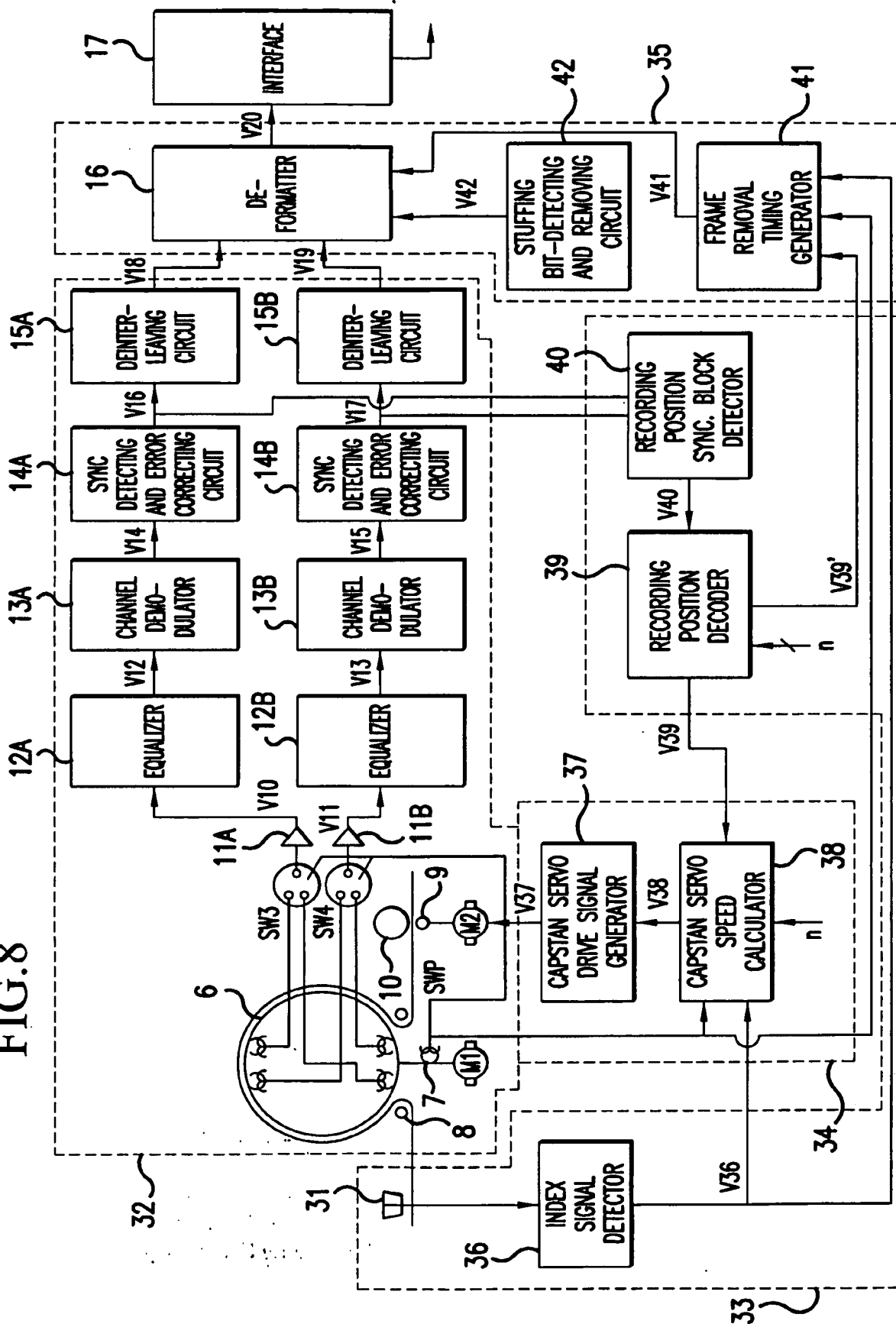


FIG.9



The diagram illustrates a video recording system architecture. It is organized into three primary functional blocks: 18 (Recording Section), 19 (Control Section), and 20 (Interface/Buffer Section).
 - **Block 18 (Recording Section):** This section handles the data flow from the interface to the recording heads. It contains an INTERLEAVING AND CHANNEL DIVIDING CIRCUIT (2) which splits the input signal into two paths. Each path goes through a RECORDING FORMATTER (3A and 3B) and a CHANNEL MODULATOR (4A and 4B). Switches SW1 and SW2 (5A and 5B) then direct the modulated signals to the recording heads (HD1, HD2, HD3, HD4) of the HEAD (6).
 - **Block 19 (Control Section):** This section manages the recording process. It includes a FRAME POSITION RECORDER (29) and an INDEX SIGNAL RECORDER (30). A TRACK NUMBER CALCULATOR (28) provides timing information (V28) to a MULTIPLEXING TIMING GENERATOR (27). The timing generator (27) also receives signals from the recording formatters (3A, 3B) and controls the switches (5A, 5B).
 - **Block 20 (Interface/Buffer Section):** This section acts as a buffer and interface. It includes a BUFFER (22) that receives data from the INTERFACE (1) and feeds it into the FRAME MEMORY (23). The FRAME MEMORY (23) is controlled by a FRAME DETECTOR (24) and provides data to the MULTIPLEXING TIMING GENERATOR (27) and the INTERLEAVING AND CHANNEL DIVIDING CIRCUIT (2). A BIT STUFFING CIRCUIT (26) also receives data from the FRAME MEMORY (23) and feeds into the MULTIPLEXING TIMING GENERATOR (27).
 - **External Components:** The system is connected to an INTERFACE (1) and a HEAD (6) with four heads (HD1, HD2, HD3, HD4). Various signal lines (V1 through V31, SW1, SW2, n) connect these components to the internal blocks.

FIG. 8



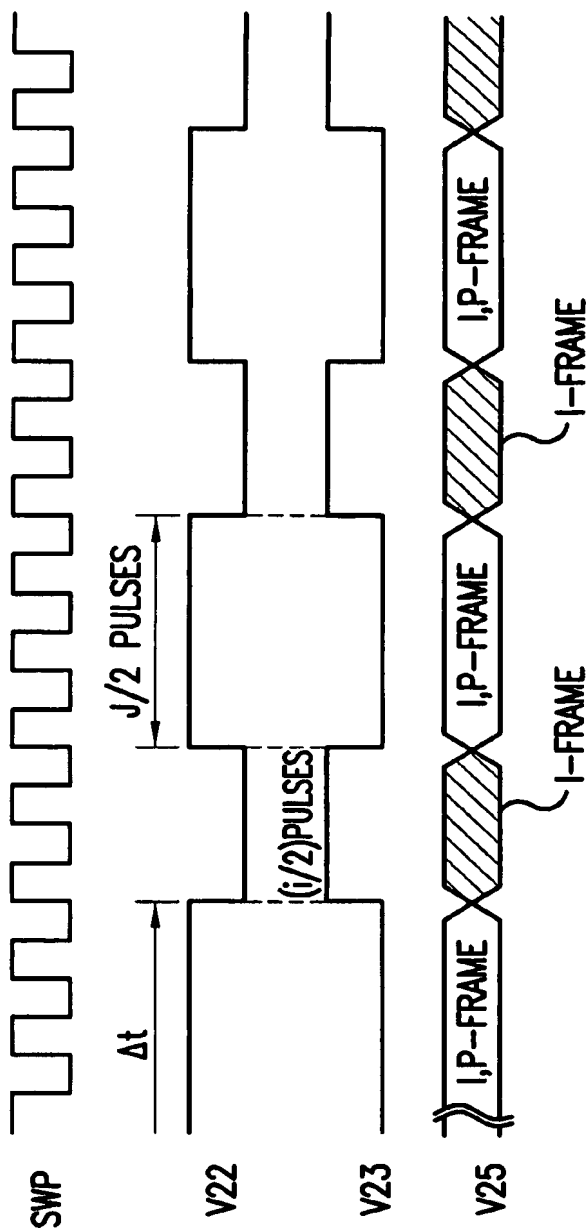


FIG.10A

FIG.10B

FIG.10C

FIG.10D

FIG.11

SYNC	ID	DIF1	DIF2	DIFn	ECC
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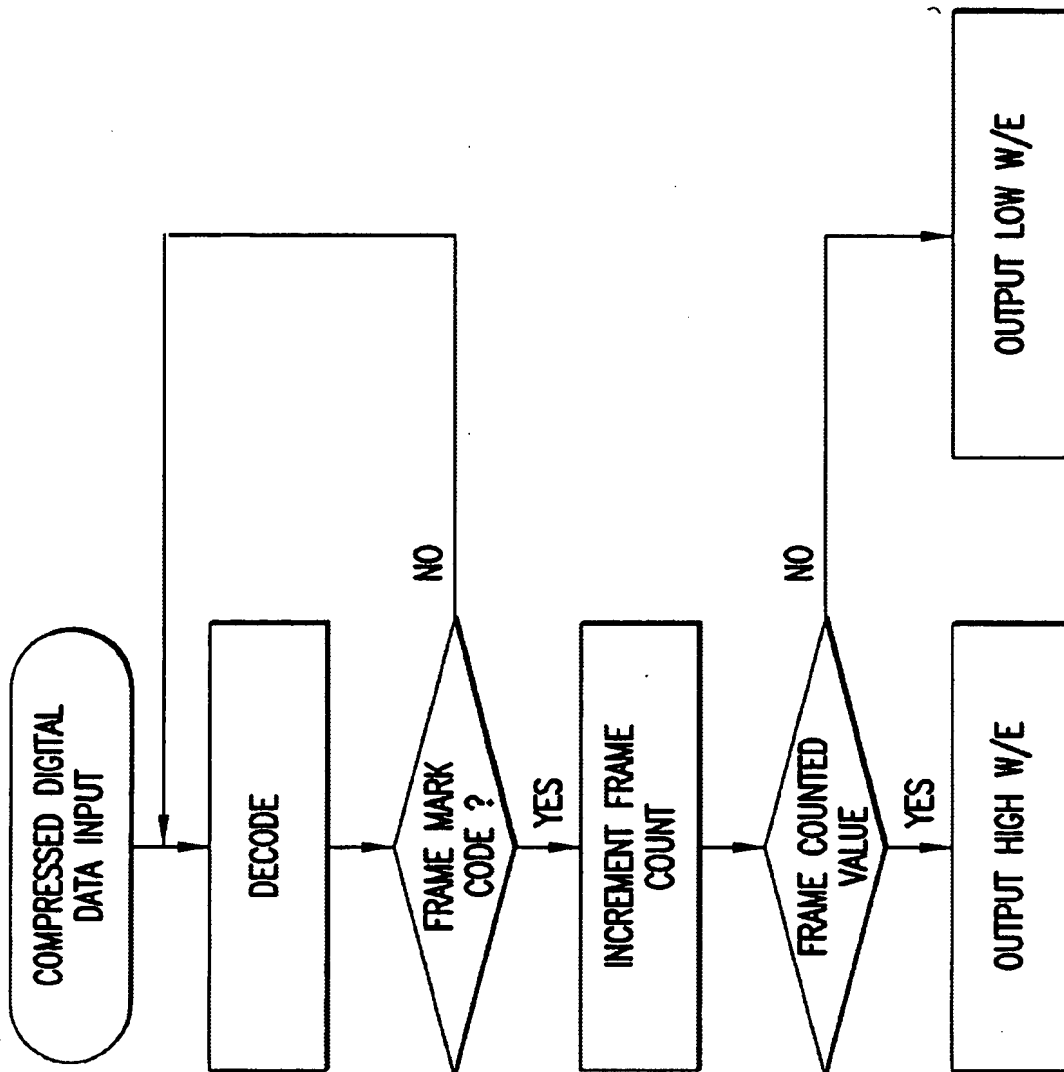


FIG.12

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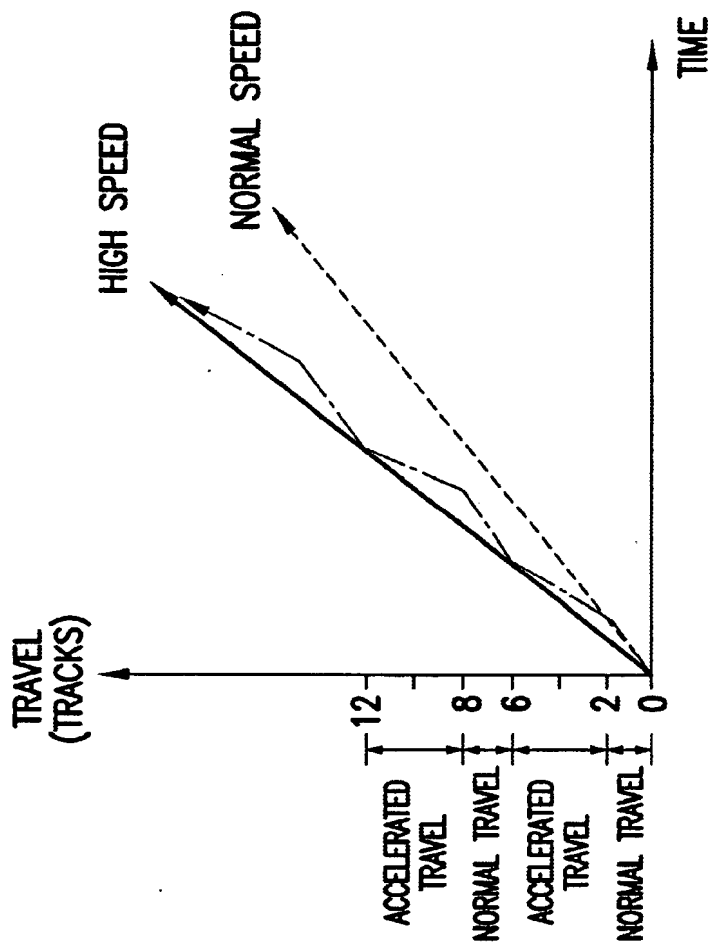


FIG.13A

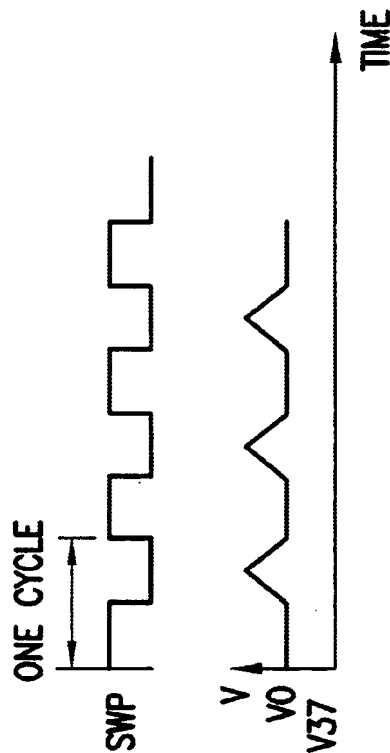
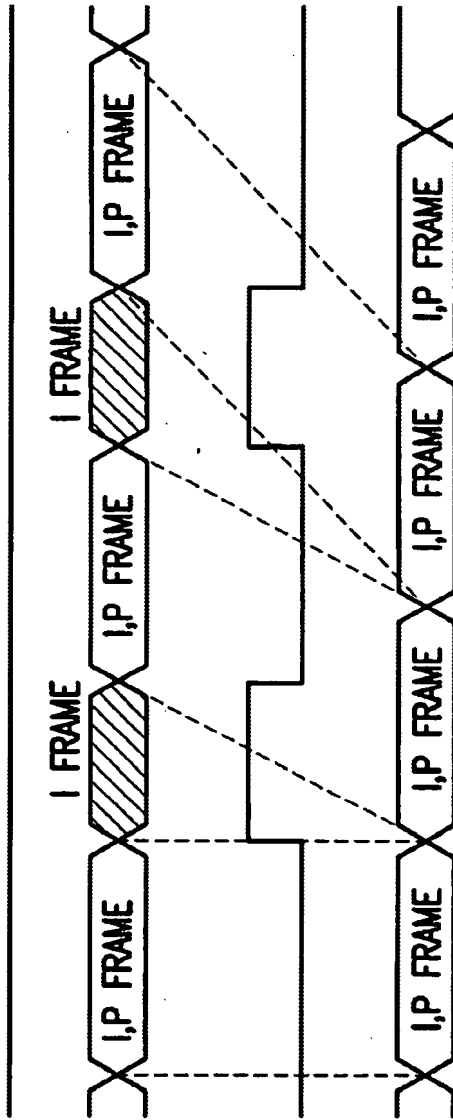


FIG.13B

FIG.13C



SWP



V18

v19

141

V20

FIG. 14A

FIG. 14B

FIG. 14C

FIG. 14D